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**Sequence 110****X10202\_en**

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Design a sequential circuit with one binary input and one binary output. The output must be 1 at cycle  $i$  when the inputs at cycles  $i - 2$ ,  $i - 1$  and  $i$  are 110, otherwise the output must be 0.

**Specification**

```
module find110(in, out, clk, rst);
    input in, clk, rst;
    output out;
```

**Hint**

The state machine can be implemented with 3 states.

**Input**

- $clk$  is the clock signal
- $rst$  is the synchronous reset signal.
- $in$  is the binary input.

**Output**

- $out$  is the output that behaves according to the specification.

**Problem information**

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