Last two equal X71700_en

Design a circuit that reads an input sequence and generates an output indicating whether the current value of the input is equal to the value at the previous cycle.

After reset, the circuit assumes that the previous value was a 0. Here is an example of an input and output sequence:

```
in:    0 1 1 1 0 1 0 1 0 0 1 1 0 0 0 1 0 1 1 0 ...
out:   1 0 1 1 0 0 0 0 0 1 0 1 0 1 1 0 0 0 1 0 ...
```

Specification

```
module last_two_equal (in, out, clk, rst);
    input in, clk, rst;
    output out;
```

Input

- *in* receives the input sequence.
- *clk* is the clock signal.
- *rst* is the synchronous reset signal.

Output

- *out* generates the output sequence.

Problem information

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Generation : 2013-09-02 15:59:06